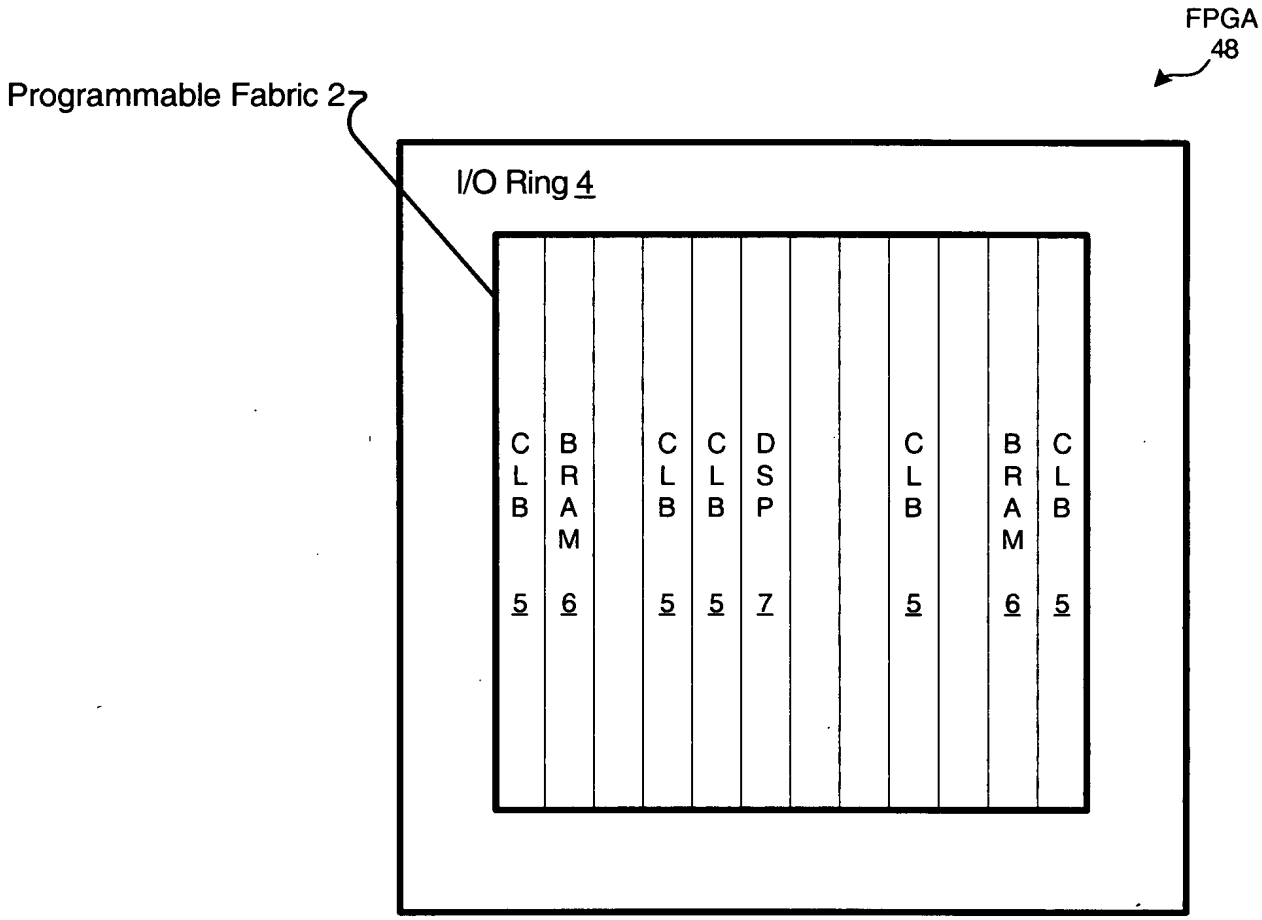

FIG. 1
(Prior Art)

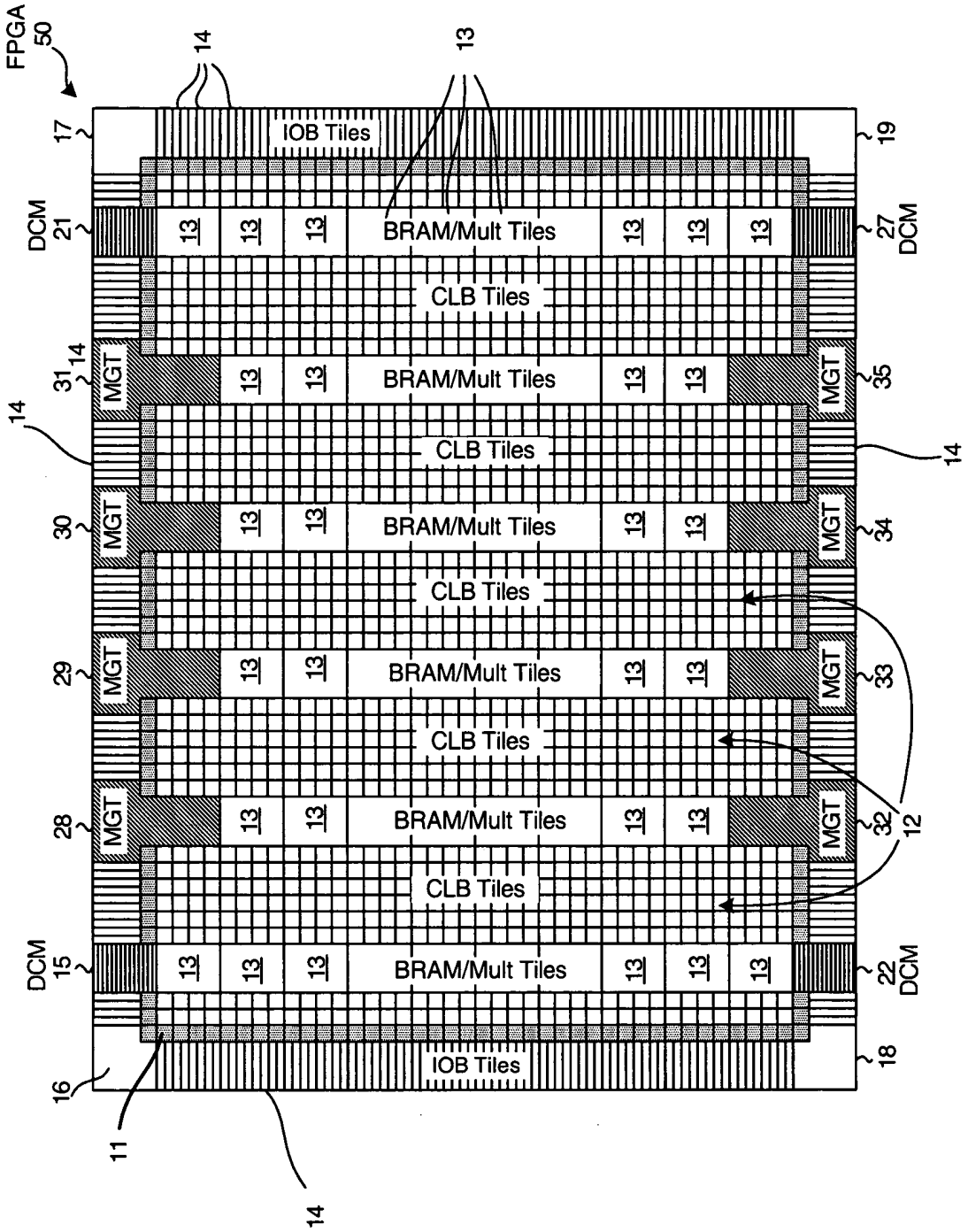

FIG. 2
(Prior Art)

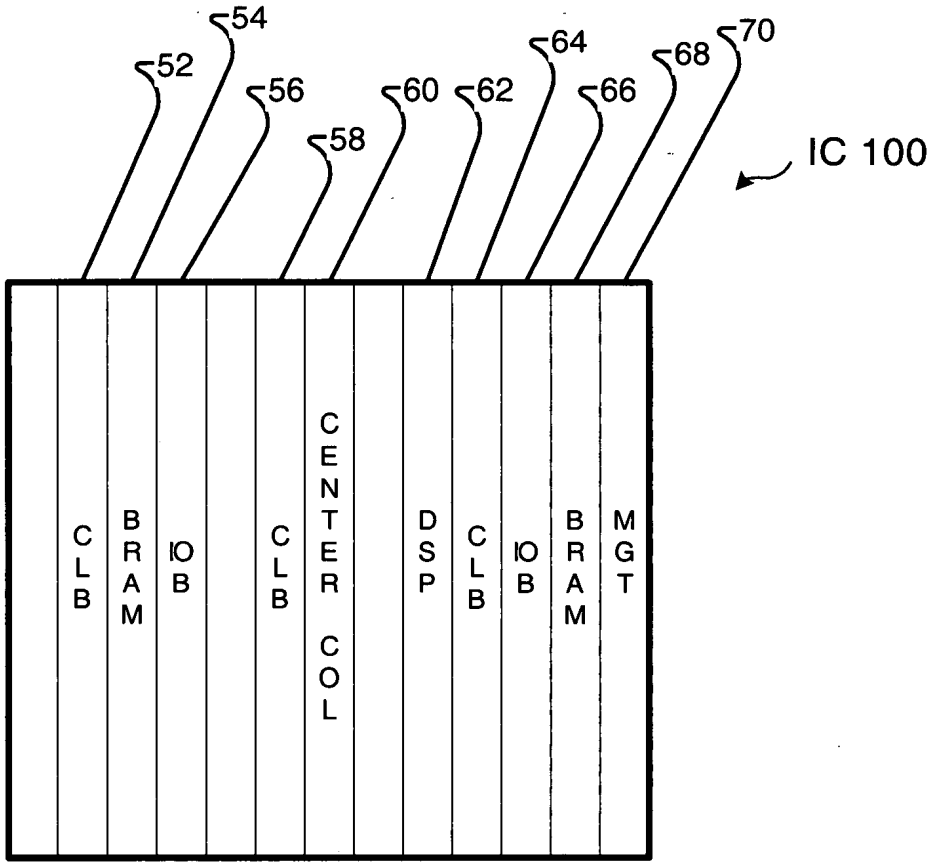
52
54
56
58
60
62
64
66
68
70
IC 100
CLB
BRAM
IOB
CLB
CENTER COL
DSP
CLB
IOB
BRAM
MGT

FIG. 3

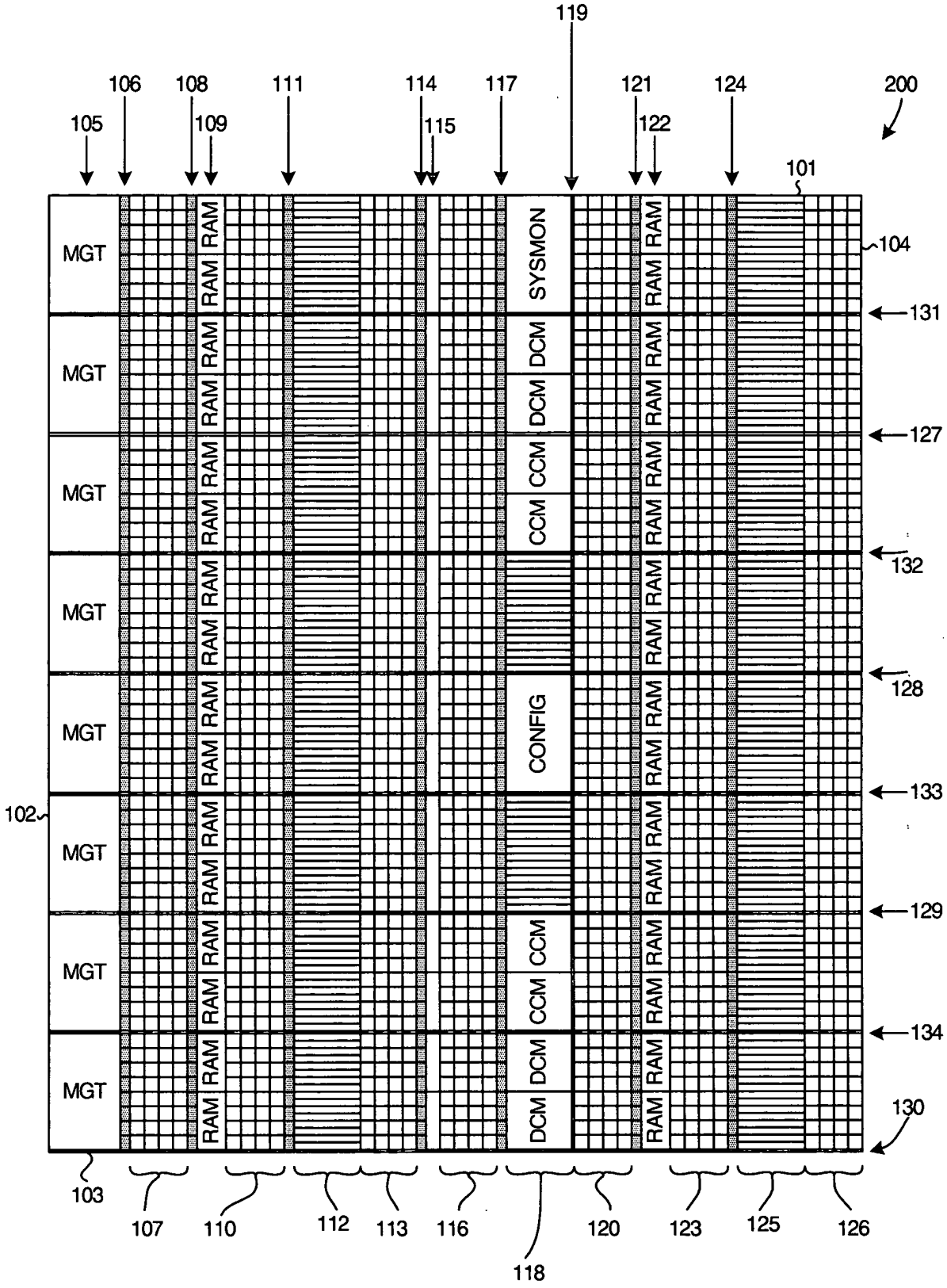
119
106
108
111
114
117
121
124
200
105
109
115
122
101
MGT
RAM
SYSMON
104
131
DCM
127
CCM
132
128
CONFIG
133
102
129
134
130
103
107
110
112
113
116
118
120
123
125
126

FIG. 4

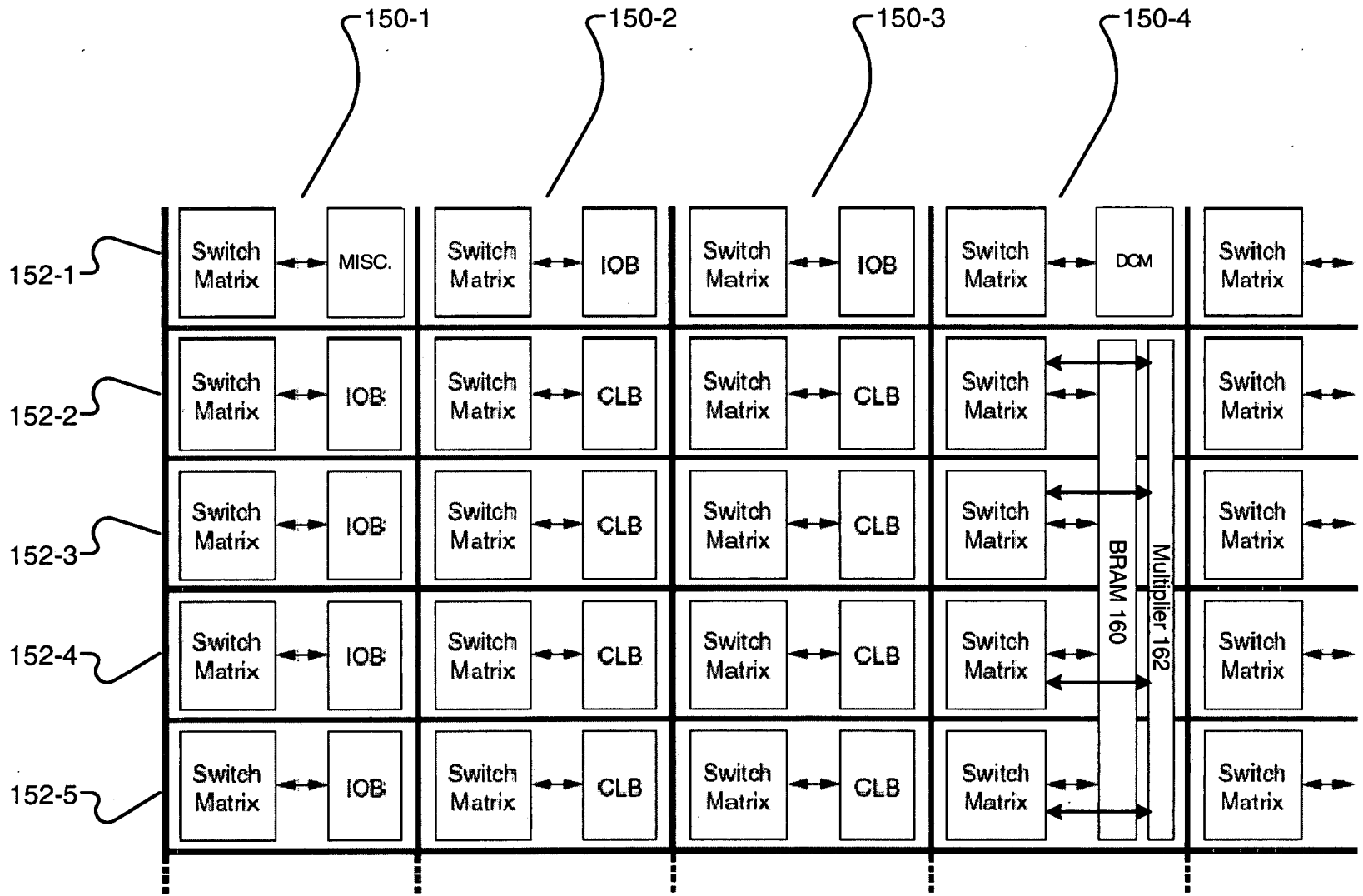

FIG. 5 (PRIOR ART)

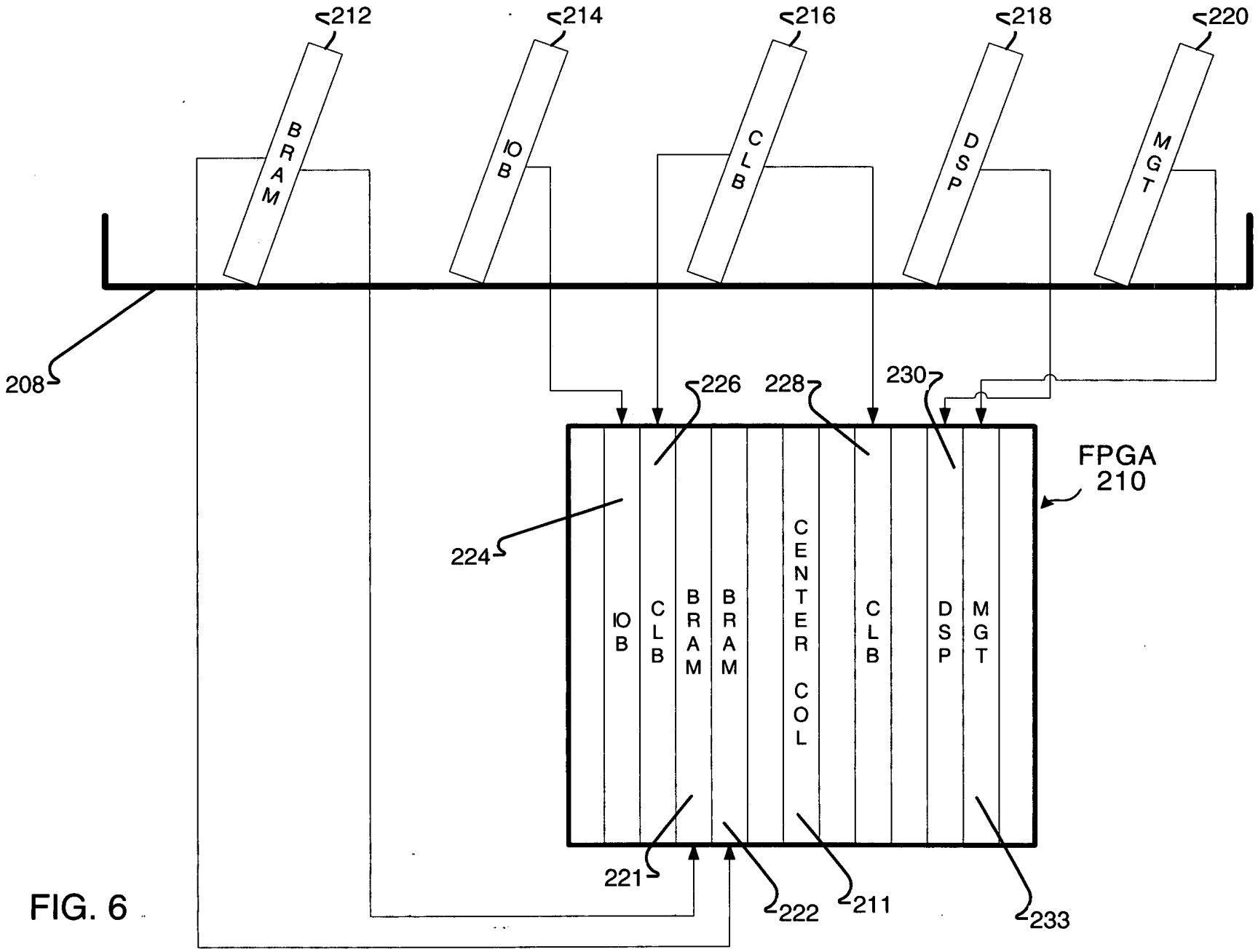
212
214
216
218
220
BRAM
IOB
CLB
DSP
MGT
208
226
228
230
FPGA
210
224
IOB
CLB
BRAM
BRAM
CENTER COL
CLB
DSP
MGT
221
222
211
233

FIG. 6

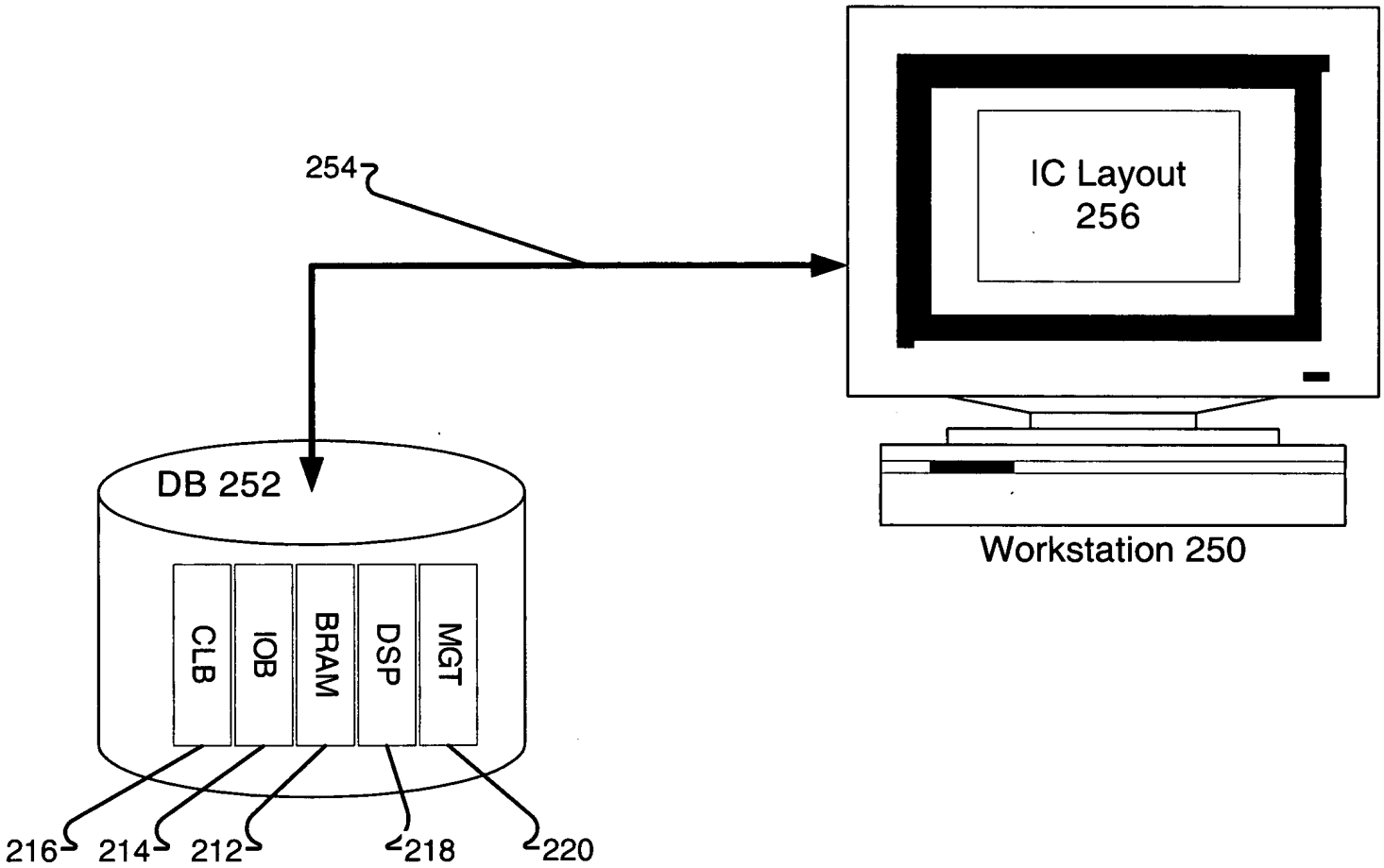
254
IC Layout
256
DB 252
CLB
IOB
BRAM
DSP
MGT
Workstation 250
216
214
212
218
220

FIG. 7

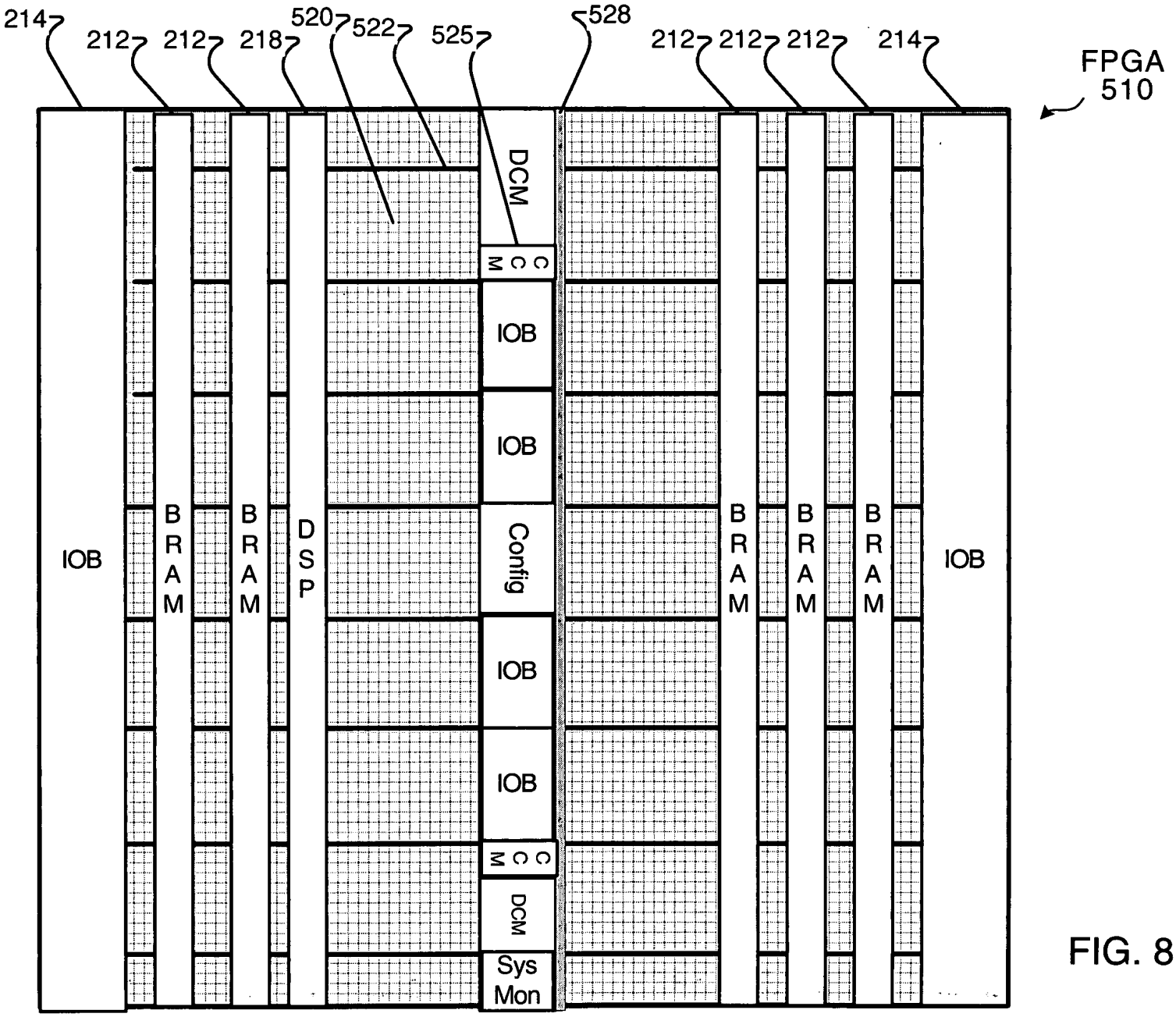
214
212
212
218
520
522
525
528
212
212
212
214
FPGA
510
IOB
BRAM
BRAM
DSP
DCM
CCM
IOB
IOB
Config
IOB
IOB
CCM
DCM
Sys Mon
BRAM
BRAM
BRAM
IOB

FIG. 8

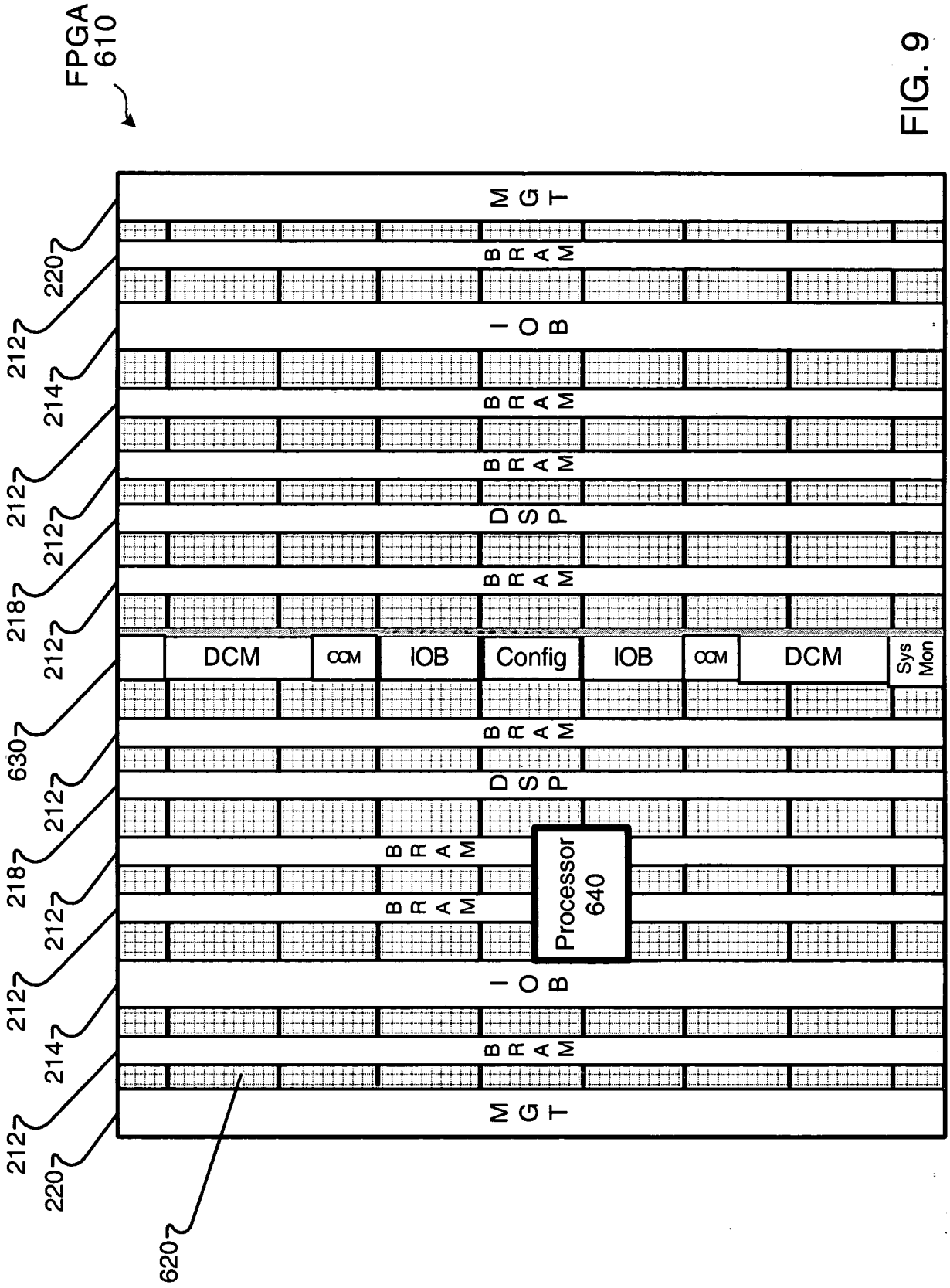
FPGA
610
620
212
220
214
218
630
MGT
BRAM
IOB
DSP
DCM
CCM
Config
Sys Mon
Processor
640

FIG. 9

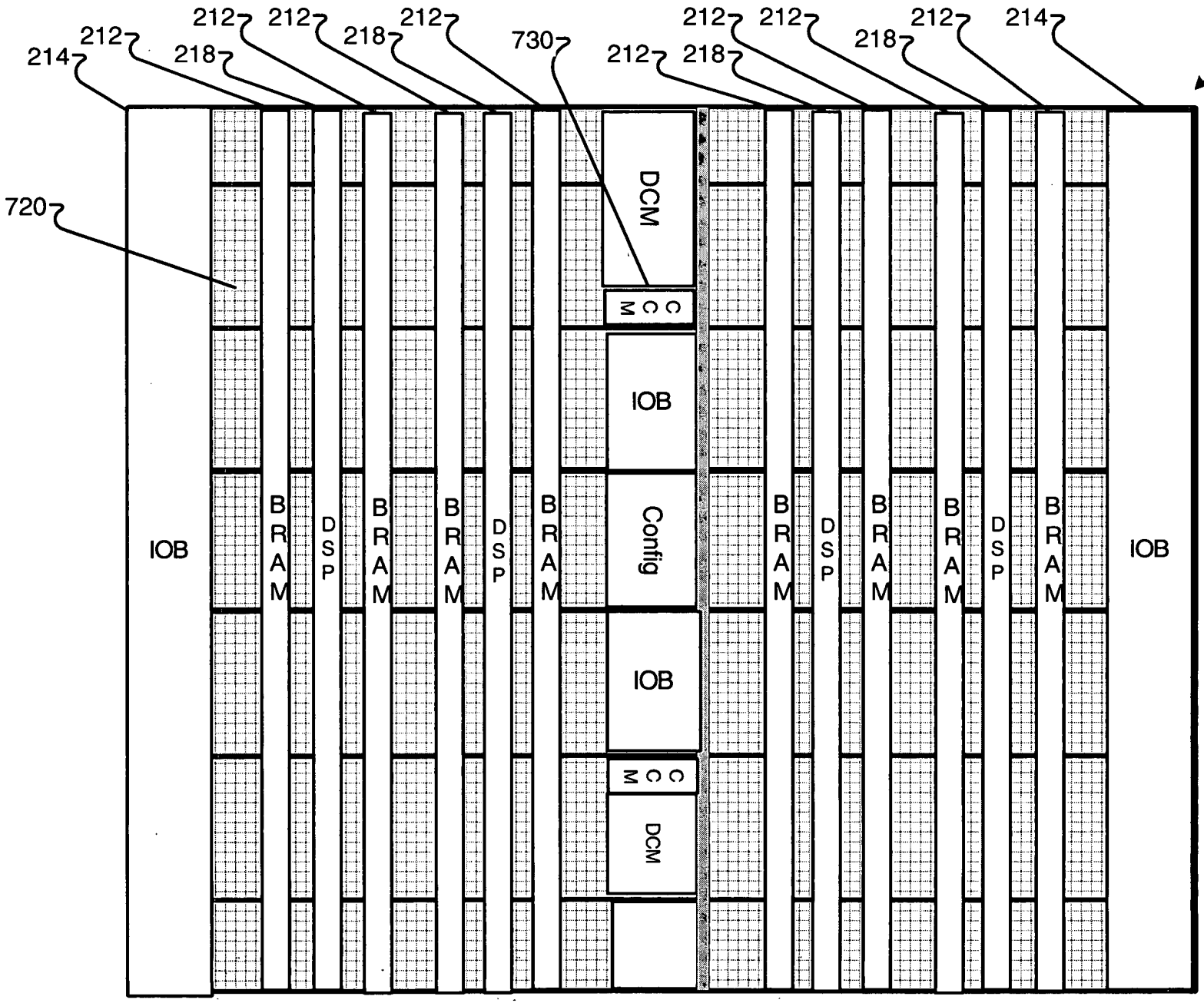

FIG. 10